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Attorney Docket No. 5649-1258

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Joo et al.

U.S. Patent No.: 7,052,951

Application Serial No.: 10/776,394

Issued: May 30, 2006

Filed: February 11, 2006

For: METHODS FOR FABRICATING FERROELECTRIC MEMORY DEVICES
WITH ENHANCED FERROELECTRIC PROPERTIES

Date: September 12, 2006

Commissioner for Patents

Attn: Certificate of Correction Branch

P.O. Box 1450

Alexandria, VA 22313-1450

**REQUEST FOR ENTRY OF CERTIFICATE OF CORRECTION UNDER
35 U.S.C §254 AND 37 C.F.R. §1.322**

Sir:

The Assignee of record for the above-referenced patent hereby requests, pursuant to 35 U.S.C §254 and 37 C.F.R. §1.322, that a Certificate of Correction be issued. This request is made in order to correct the mistakes incurred through the fault of the U.S. Patent and Trademark Office. No fee is believed due. However, the Commissioner is authorized to charge any deficiency or credit any overpayment to Deposit Account No. 50-0220.

The mistakes appearing in the patent are set forth with corrections on the Certificate of Correction enclosed herewith, with an additional copy thereof and a return post card.

Respectfully submitted,

D. Randal Ayers
Registration No. 40,493

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**Certificate
SEP 18 2006
of Correction**

Certificate of Mailing under 37 CFR 1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, Attn: Certificate of Correction Branch, P.O. Box 1450, Alexandria, VA 22313-1450 on September 12, 2006.

Jessica M. French

SEP 19 2006

UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

PATENT NO. : 7,052,951
DATED : May 30, 2006
INVENTOR(S) : Joo et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the Title Page.

Section 54 should read -- METHODS FOR FABRICATING FERROELECTRIC MEMORY DEVICES WITH ENHANCED FERROELECTRIC PROPERTIES --

Column 1.

Lines 1-4 should read -- METHODS FOR FABRICATING FERROELECTRIC MEMORY DEVICES WITH ENHANCED FERROELECTRIC PROPERTIES --

Column 11.

Line 59 should read -- surface of the upper insulating pattern is higher than a --

Column 12.

Line 1 should read -- after patterning the lower electrode layer, the ferroelectric layer and the upper electrode layer, forming a third --

Line 32 should read -- sequentially stacked iridium and titanium aluminum nitride --

Column 13.

Line 5 should read -- forming a lower insulating layer including a conductive plug --

Line 9 should read -- patterning the upper insulating layer to form an opening --

Line 45 should read -- 19. The method of claim 15, wherein forming a lower --

Column 14.

Line 52 should read -- after patterning the lower electrode layer, the ferroelectric layer and the upper electrode layer, forming a third --

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PATENT NO. 7,052,951

No. of additional copies: _____



This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you are required to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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